In the Claims:

1. (Cancelled)

2. (Currently Amended) The MOS transistor of Claim 6,[[1,]] further comprising an insulating gate spacer covering the first and second sidewalls of the silicon column portion of the inverted T-shaped gate electrode, wherein the second lightly-doped drain region and the second lightly-doped source region are under bottom portions of the insulating gate spacer.

3. (Original) The MOS transistor of Claim 2, wherein the heavily doped drain region is adjacent a first outer sidewall of the insulating gate spacer and wherein the heavily doped source region is adjacent a second outer sidewall of the insulating gate spacer.

4. (Currently Amended) The MOS transistor of Claim 2, wherein a bottom surface of the insulating gate spacer is on ~~a~~ the curing thermal oxide layer.

5. (Cancelled).

6. (Currently Amended) A MOS transistor comprising:

an inverted T-shaped gate electrode on a substrate, the inverted T-shaped gate electrode comprising a silicon base portion and a silicon column portion extending from the base portion, the silicon base portion and the silicon column portion doped with a same dopant material, the silicon base portion of the inverted T-shaped gate electrode including a first lateral protrusion extending laterally beyond a first sidewall of the silicon column portion of the inverted T-shaped gate electrode and a second lateral protrusion extending laterally beyond a second sidewall of the silicon column portion of the inverted T-shaped gate electrode;

a drain region in the substrate comprising a first lightly-doped drain region under the first lateral protrusion, a second lightly-doped drain region that is deeper than the first lightly-doped drain region adjacent the first lightly-doped drain region, and a heavily-doped drain region adjacent to the second lightly-doped drain region;

a source region in the substrate comprising a first lightly-doped source region under the second lateral protrusion, a second lightly-doped source region that is deeper than the first lightly-doped source region adjacent the first lightly-doped source region, and a heavily-doped source region adjacent to the second lightly-doped source region;

a gate dielectric layer interposed between the inverted T-shaped gate electrode and the substrate; and

~~The MOS transistor of Claim 5, further comprising~~ a curing thermal oxide layer on the first and second sidewalls of the silicon column portion of the inverted T-shaped gate electrode, the first and second sidewalls of the gate dielectric, the second lightly-doped drain region and the second lightly-doped source region,

wherein a first sidewall of the gate dielectric is aligned with a sidewall of the first lateral protrusion of the inverted T-shaped gate electrode and wherein a second sidewall of the gate dielectric is aligned with a sidewall of the second lateral protrusion of the inverted T-shaped gate electrode.

7. (Currently Amended) The MOS transistor of Claim 6, ~~wherein the~~ further comprising an insulating gate spacer ~~is~~ on the curing thermal oxide layer.

8. (Original) The MOS transistor of Claim 7, further comprising a spacer etch stop layer interposed between the insulating gate spacer and the curing thermal oxide layer.

9. (Currently Amended) The MOS transistor of Claim 6,[[1,]] wherein the sidewalls of the first and second lateral protrusions are vertically profiled.

10. (Withdrawn—Currently Amended) The MOS transistor of Claim 6,[[1,]] wherein the sidewalls of the first and second lateral protrusions are sloped at positive angles.

11. (Withdrawn—Currently Amended) The MOS transistor of ~~claim 1~~ Claim 6, wherein the sidewalls of the first and second lateral protrusions are sloped at negative angles.

12. (Currently Amended) The MOS transistor of Claim 6, ~~claim 1~~ further comprising a metal silicide layer on the upper surface of the inverted T-shaped gate electrode, the surface of the heavily-doped drain region and the surface of the heavily-doped source region.

13-53. (Cancelled)

54. (Currently Amended) The MOS transistor of Claim 6,[[5,]] wherein the depth of the second lightly-doped drain region is about the same as the combined depth of the first lightly-doped drain region, the gate dielectric layer and the silicon base portion of the inverted T-shaped gate electrode.

55. (Currently Amended) The MOS transistor of Claim 6,[[1,]] wherein the silicon base portion and the silicon column portion of the inverted T-shaped gate electrode are not selectively etchable.